

IN THE CLAIMS:

CLAIMS

Please cancel claims 3, 21, 36.

Please amend the claims as follows:

1. (Once Amended) An interface to transfer data directly between a first hub and a second hub within a computer system, comprising:
a data signal path to transmit data in packets via split transactions; and
a set of command signals, wherein said interface provides a point-to-point connection between said first hub and said second hub, exclusive of an external bus connected directly to the interface.

3. (Canceled)

19. (Once Amended) An interface to transfer data directly between a first hub and a second hub within a computer system, comprising:
a first means for transmitting data between said first hub and said second hub in packets via split transactions; and
a second means for transmitting command signals, wherein said interface provides a point-to-point connection between said first hub and said second hub, exclusive of an external bus connected directly to the interface.

21. (Canceled)

35. (Once Amended) An interface to transfer data between a first hub and a second hub within a computer system, comprising:
a set of data signals and a pair of source synchronous strobe signals, said data signals transmit data in packets via split transactions, said packets including a request

5 < packet and completion packet, said request packet including a transaction descriptor;

6 and

7 a set of command signals including unidirectional arbitration signal and a
8 common clock signal, wherein said interface provides a point-to-point connection
9 between said first hub and said second hub, exclusive of an external bus connected
10 directly to the point-to-point connection.

1 36. (Canceled)

sub 1 37. An interface to transfer data between a memory controller hub and an input/output
2 (I/O) hub of a chipset within a computer system, comprising:

3 a bi-directional data signal path and a pair of source synchronous strobe signals,
4 said data signal path transmits data in packets via split transactions, said packets
5 including a request packet and completion packet, said request packet including a
6 transaction descriptor ; and

7 a set of command signals including unidirectional arbitration signal, a bi-
8 directional stop signal, a system reset signal, a common clock signal, and a voltage
9 reference signal.